

# Block of Low Gain

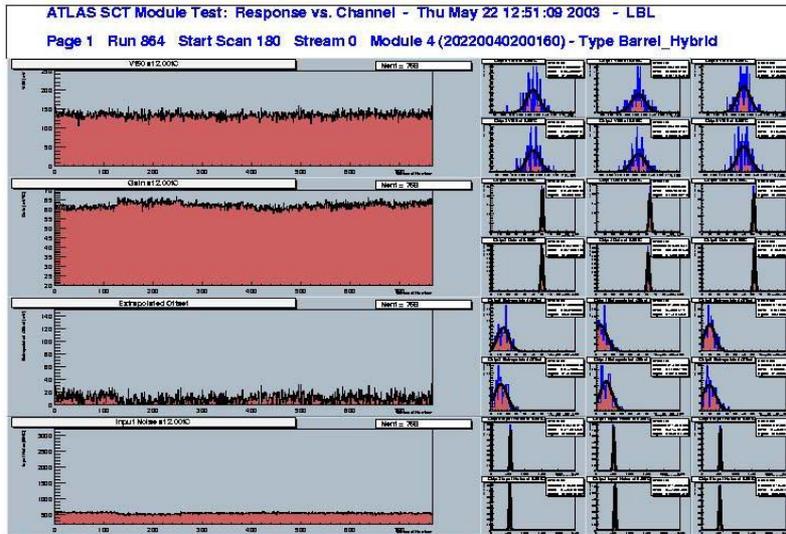
Analysis and Solutions

A. Ciocio - LBNL

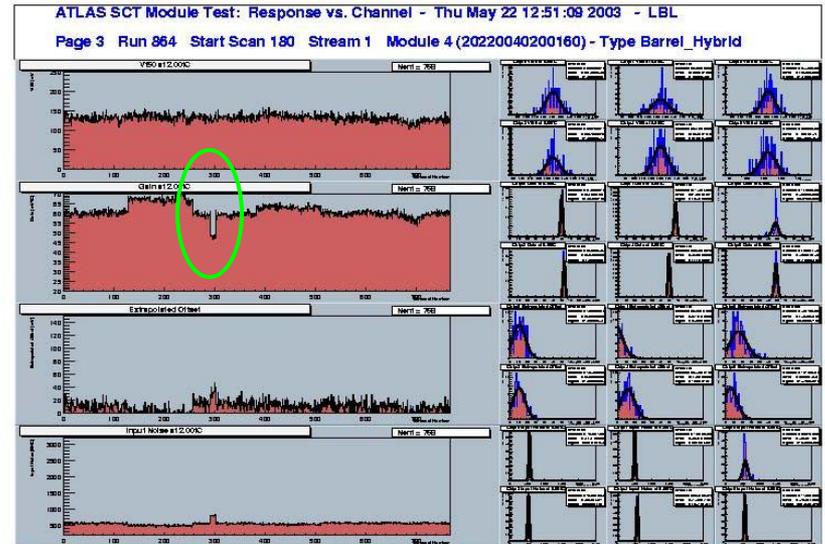
# Block Low Gain – Hybrid 00160

- Block of contiguous channels with 10-20% lower gain
- Difference in gain enhanced (in most cases) at cold temperature
- Standard test FAIL because of the high-noise consecutive channels associated with the low gain of BLG channels
- Chips that show this effect are mostly coming from lot **Z41032** and Z40920

Z40859	1
Z40920	9
<b>Z41032</b>	<b>22</b>
Z41183	3

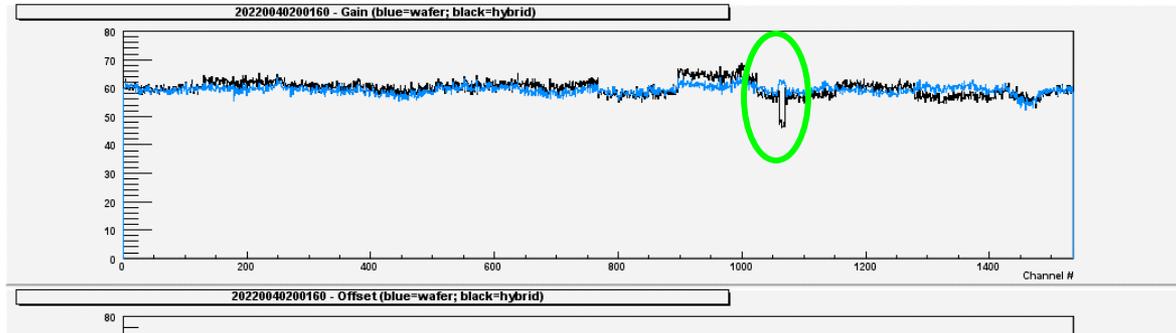


M0 S1 S2 S3 S4 E5  
16 16 16 16 16 14



M8 S9 S10 S11 S12 E13  
15 16 15 15 18 17

# Wafer/Hybrid comparison



Black = Hybrid  
Blue = Wafer

- The gain for BLG channels is actually an opposite bump at the wafer level
- Hybrid tests run the strobe delay in edge mode and all the other tests except TW in level mode
- Wafer tester runs all the tests except SD in edge-mode and we used level mode to calculate SD
- Different charge/threshold conditions

## Wafer

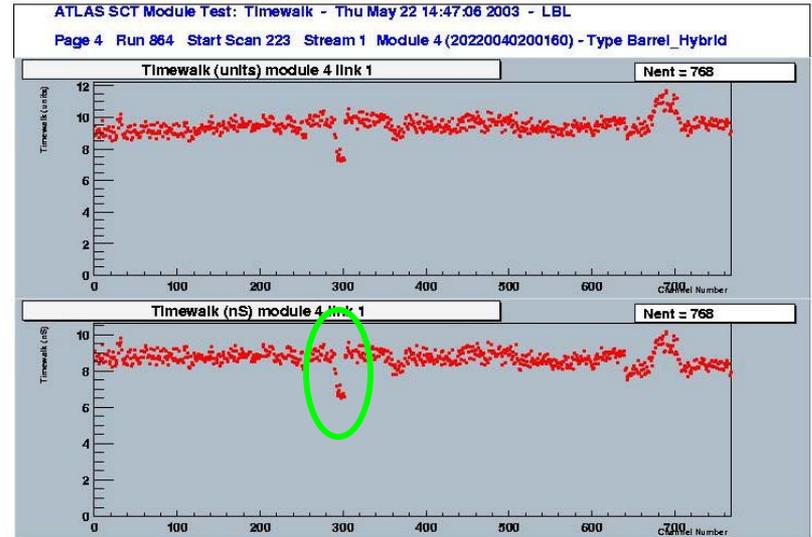
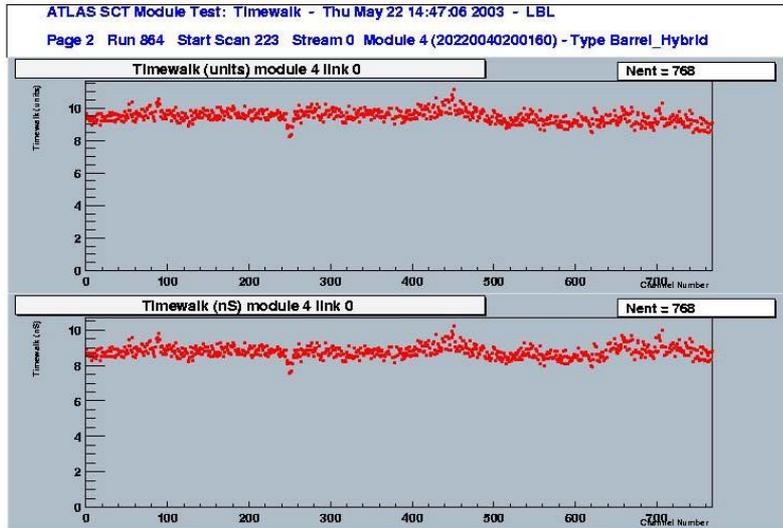
- input charge set near to threshold
- efficiency peaks at around 50%
- SD value is set to correspond to that peak
- the response is dominated by highest gain ch

## Hybrid

- gain for charges in the range 1 - 4 fC
- SD chosen for a larger range of values
- 25% between the leading and falling edge
- not intended to handle significant number of anomalous channels
- High gain channels might fall in the tail of SD

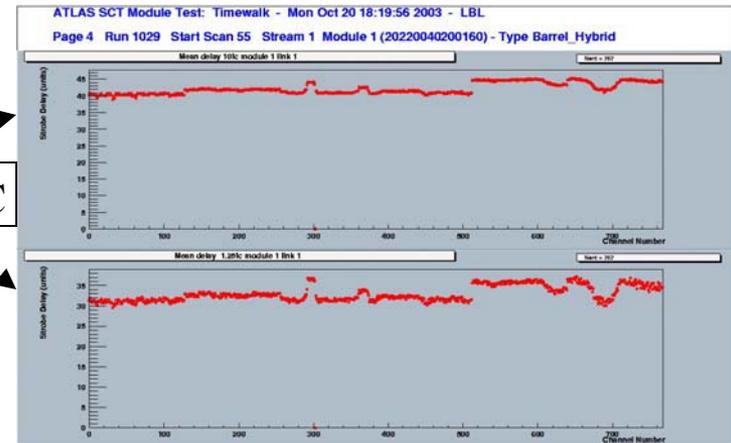
- This suggest that BLG channels might actually be High-Gain channels

# Time Walk



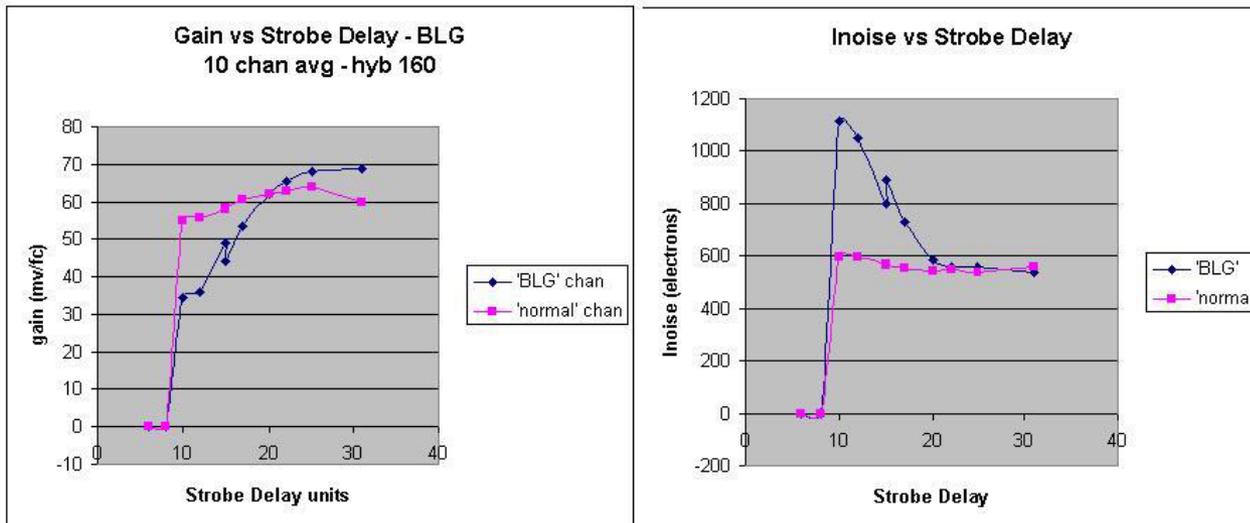
- TW for channels with BLG is clearly lower than the normal
- This suggests that BLG channels might have a faster rise time and the charge is being injected too early
- This hypothesis triggered the idea of using higher SD

Strobe delay for charge injections of  $10\text{fC}$  and  $1.25\text{fC}$   
 that are used to calculate the timewalk  
 BLG channels have larger delays



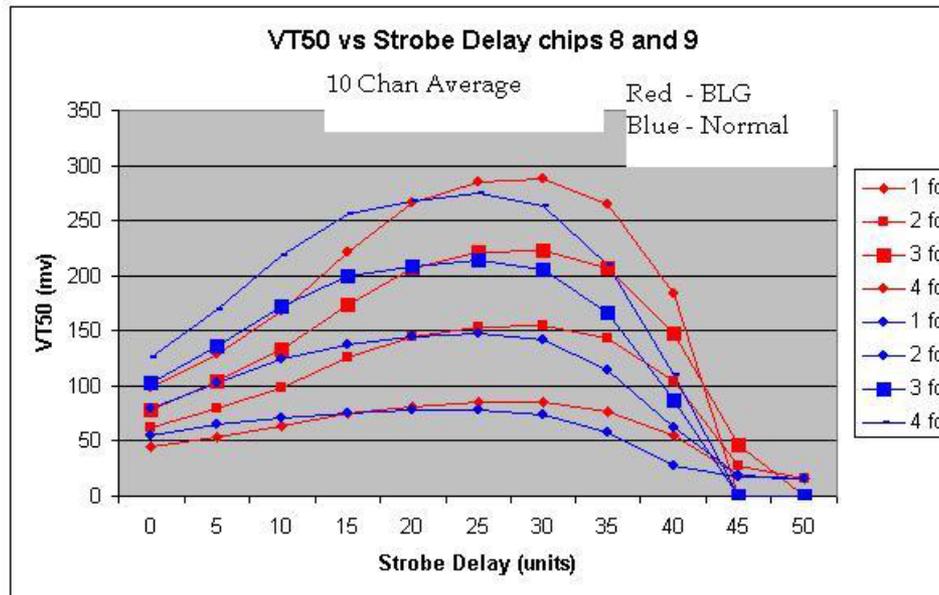
# Gain and Input Noise

- Hybrid 160 has 10 channels showing BLG in S10
- Average of the gain and the noise as a function of strobe delay for 10 BLG channels and 10 normal channels
- The excess noise becomes the same for all channels at higher SD



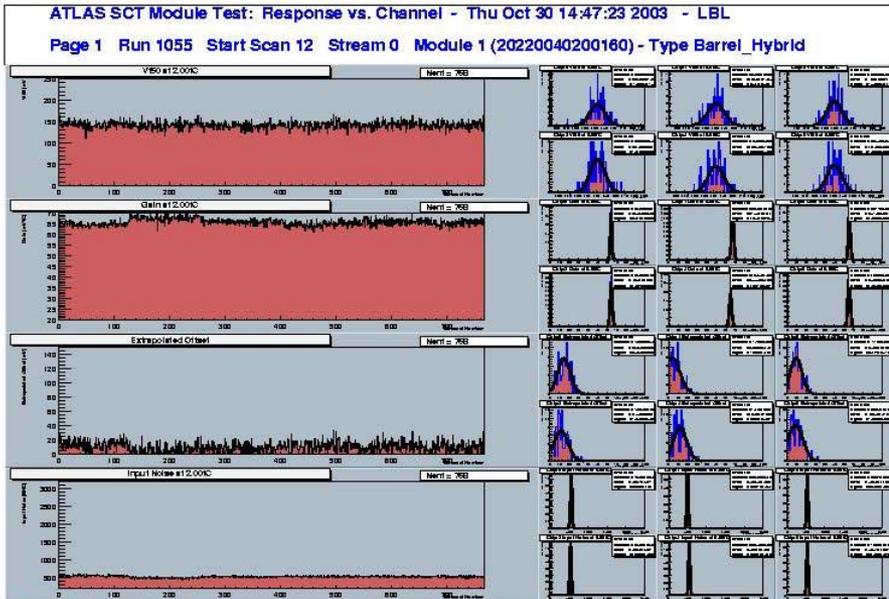
# VT50

- Average VT50 for the 10 BLG channels of Chip S10 and the corresponding 10 channels from S11 for SD from 0 to 50 and for Injected charge of 1,2,3,and 4 fC (the other chips look pretty much like S11)
- The StrobeDelay macro usual finds something around 15
- If the curves can be said to have a plateau, 20,25 and 30 look better than 15.

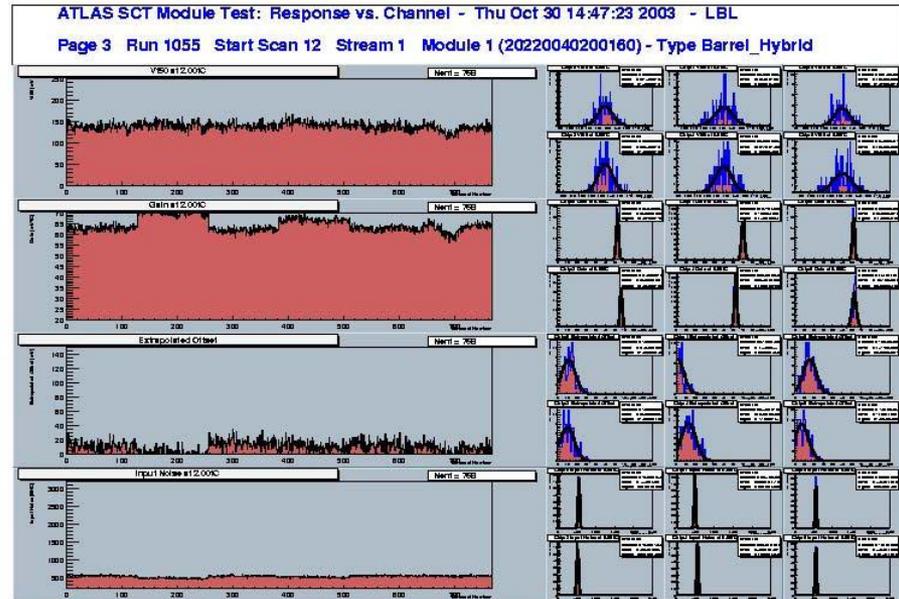


# Increased SD to 40% fraction

- Using 4.0fC signal and a threshold of 2.0fC (SD scan)
- An error function is fitted to the rising edge of a strobe delay peak (falling edge of the signal) and to the falling edge (rising edge)
- Strobe delay register is set to 25% of the distance between the two edges
- By increasing the SD as 40% of the way from the leading edge to the falling edge to accommodate high gain (or fast rise) channels which fall in the tail of the SD peak the BLG effect disappears



M0 S1 S2 S3 S4 E5  
 21 21 21 21 21 19

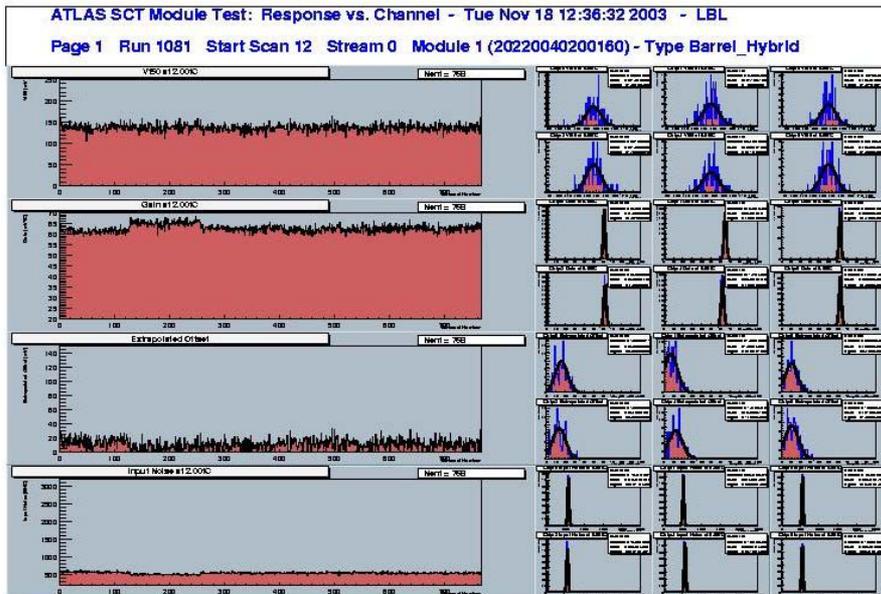


M8 S9 S10 S11 S12 E13  
 20 21 20 20 23 22

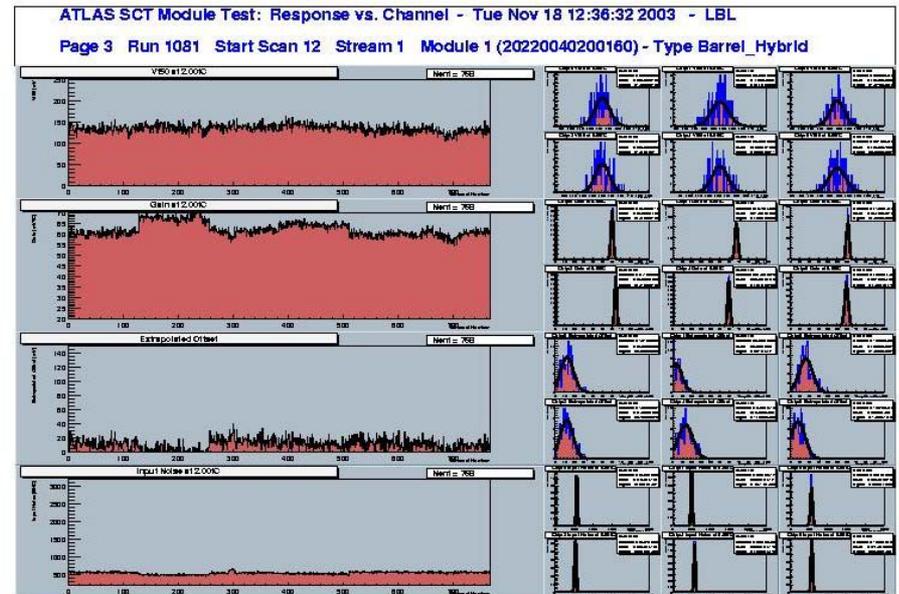
# MaxLeadingEdge-MinFallingEdge SD Algorithm RC

More complex algorithm:

- finds the max SD for the leading edge and the minimum SD for the falling edge
- calculates the strobe delay as 25% of the way from the max leading edge to the minimum falling edge
- SD is slightly bigger but enough to make the BLG effect disappears

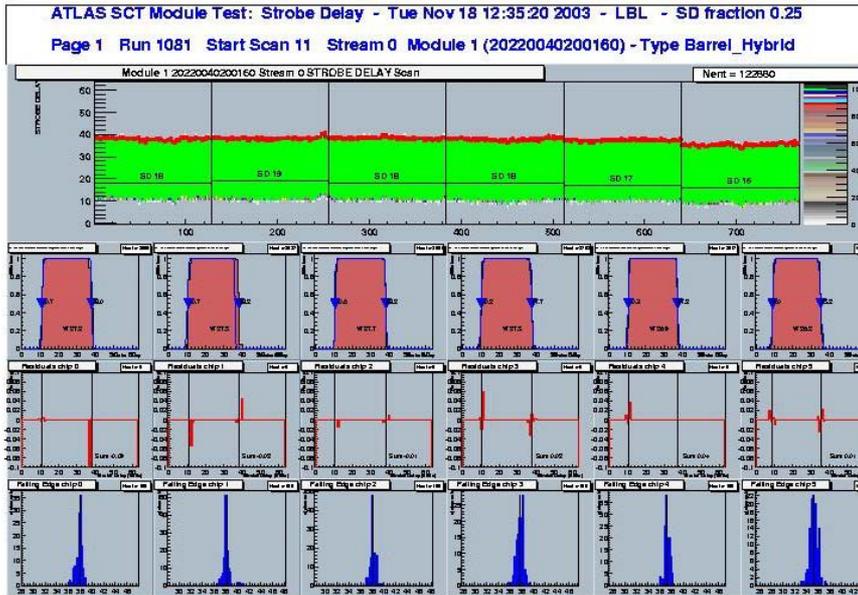


M0 S1 S2 S3 S4 E5  
18 19 18 18 17 16

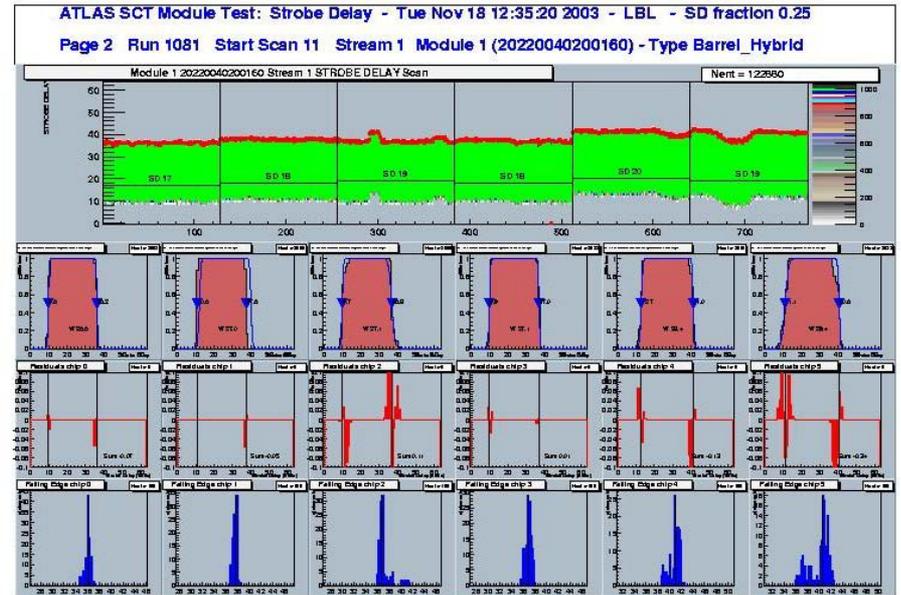


M8 S9 S10 S11 S12 E13  
17 18 19 18 20 19

# MaxLeadingEdge-MinFallingEdge SD Algorithm SD



M0 S1 S2 S3 S4 E5  
18 19 18 18 17 16

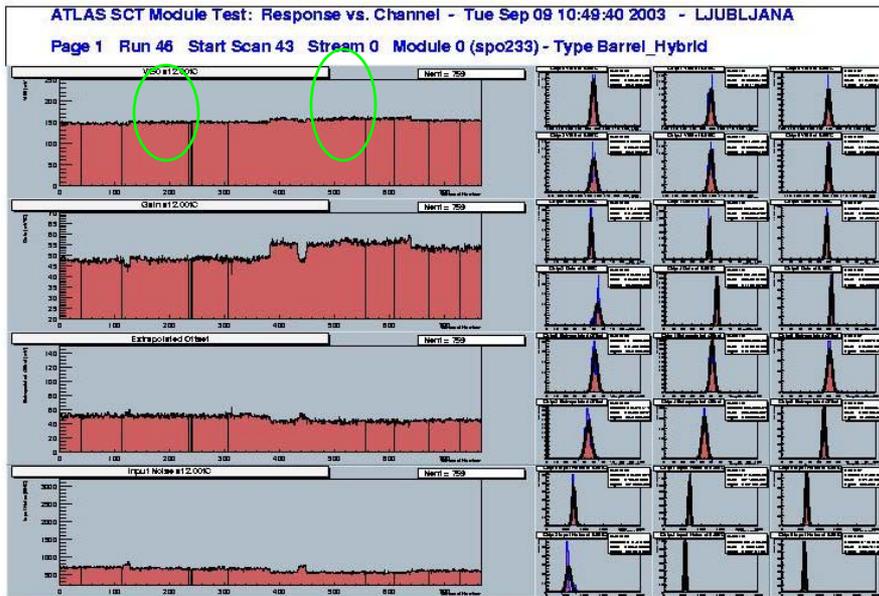


M8 S9 S10 S11 S12 E13  
17 18 19 18 20 19

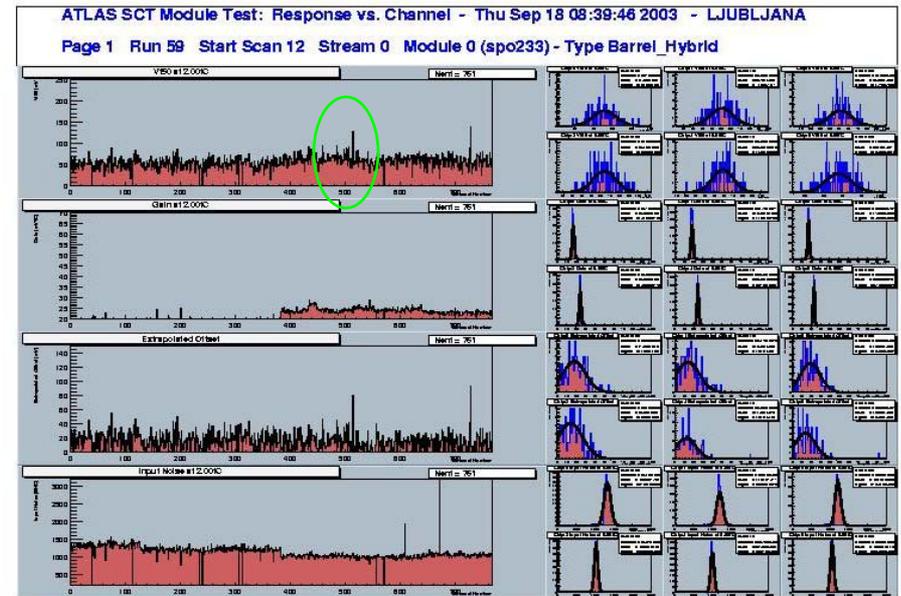
# Irradiation – RC

- To know whether the defect that causes these channels to have a faster rise time might cause other problems.
- Hybrid assembled at UCSC
- Irradiated with  $2 \times 10^{14}$  n/cm<sup>2</sup> (1 MeV NIEL equivalent in Si) in the reactor in Ljubljana (9/03)

Before Irradiation



After Irradiation



Before irradiation  $I_{Sh} = 30 \mu A$ ,  $I_{preamp} = 220 \mu A$

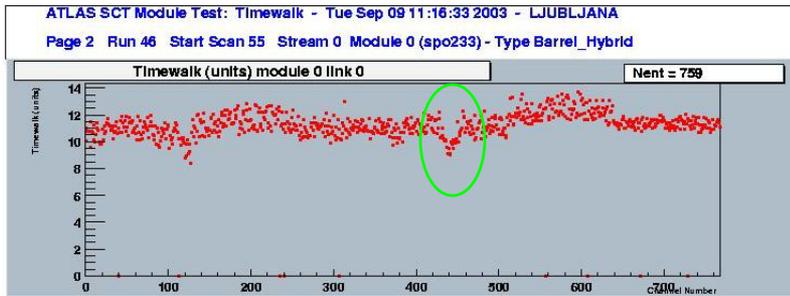
After irradiation:  $I_{Sh} = 30 \mu A$ ,  $I_{preamp} = 100 \mu A$ .

# Irradiation – Gain

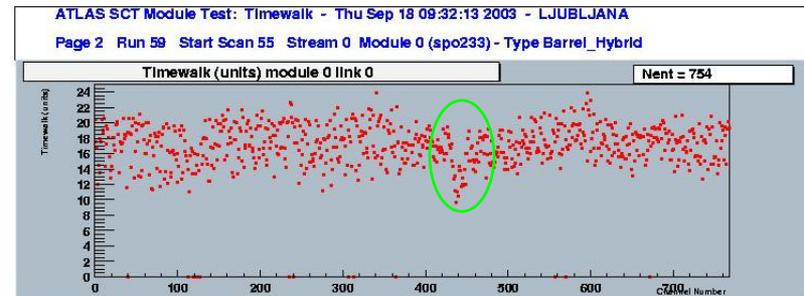
		Average Gain of LowGain channels	Average Gain of the rest of channels
M0 ch 118-127	Before Irradiation	44.66	47.60
	After Irradiation	17.35	16.25
S3 ch 433-449	Before Irradiation	48.58	55.32
	After Irradiation	24.27	23.29

# Irradiation – TW

Before Irradiation



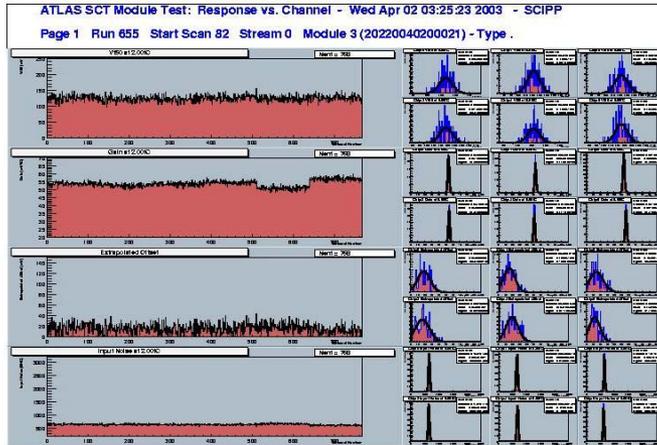
After Irradiation



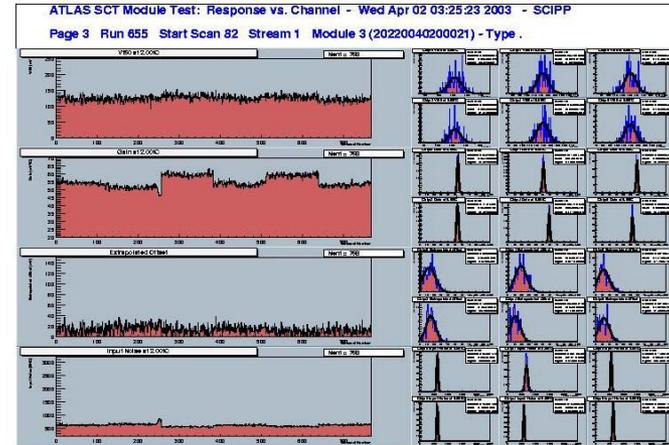
The radiation slows down the chips and causes the TW to increase uniformly  
The channel-to-channel scatter seems to be as bad as the difference in these channels before irradiation

# Module with BLG – 00021 – RC SD 40%

Hybrid  
at cold

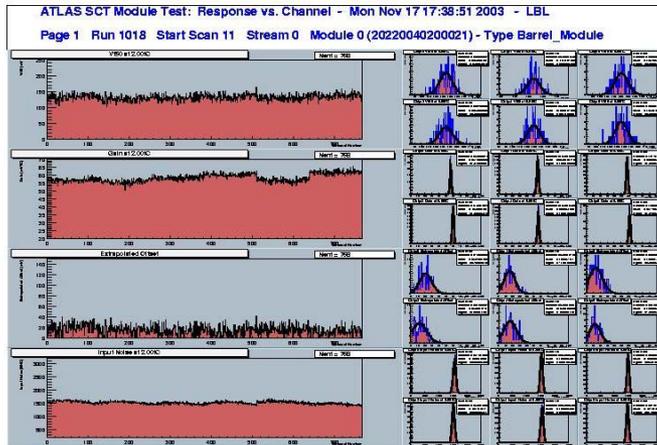


M0 S1 S2 S3 S4 E5  
17 15 15 16 16 17

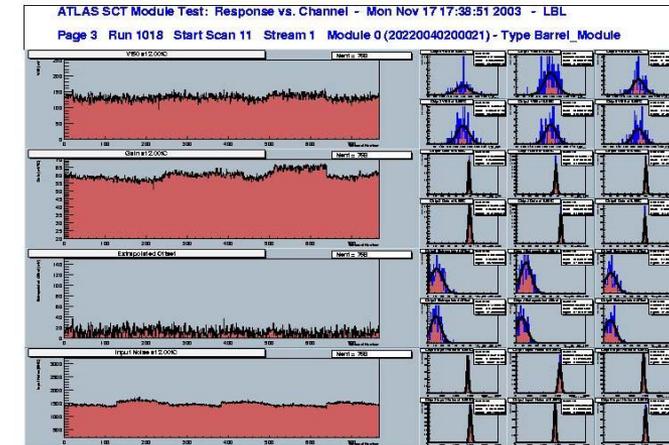


M8 S9 S10 S11 S12 E13  
17 17 19 17 17 16

Module  
SD at 40%

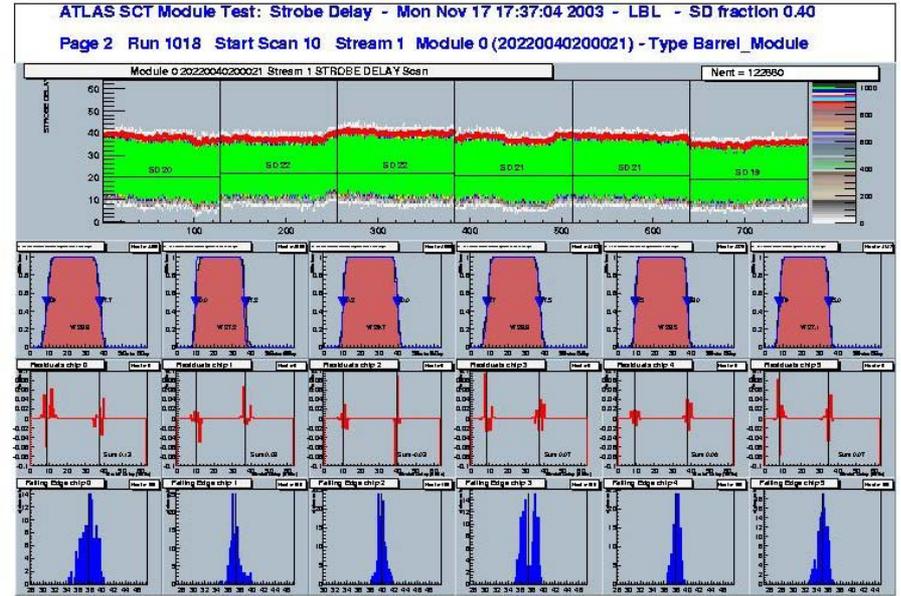
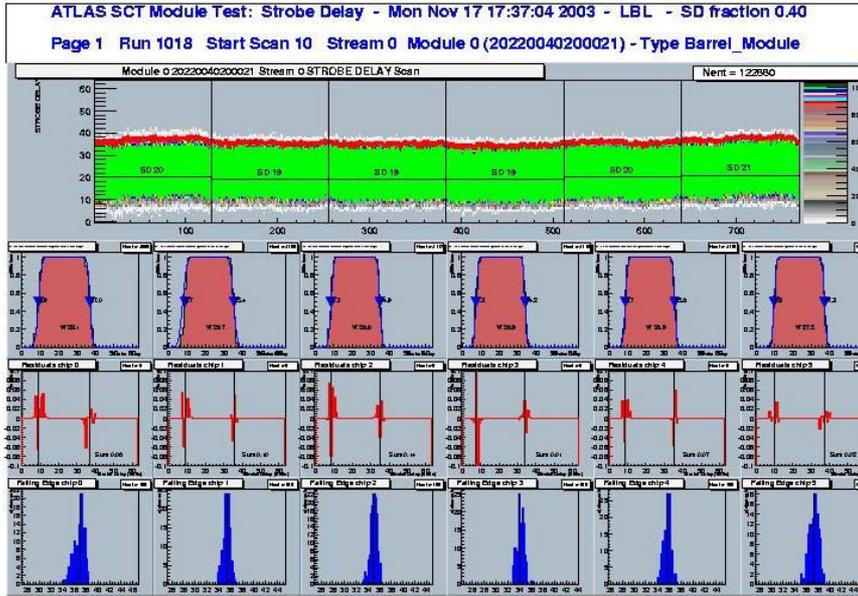


M0 S1 S2 S3 S4 E5  
20 19 19 19 20 21

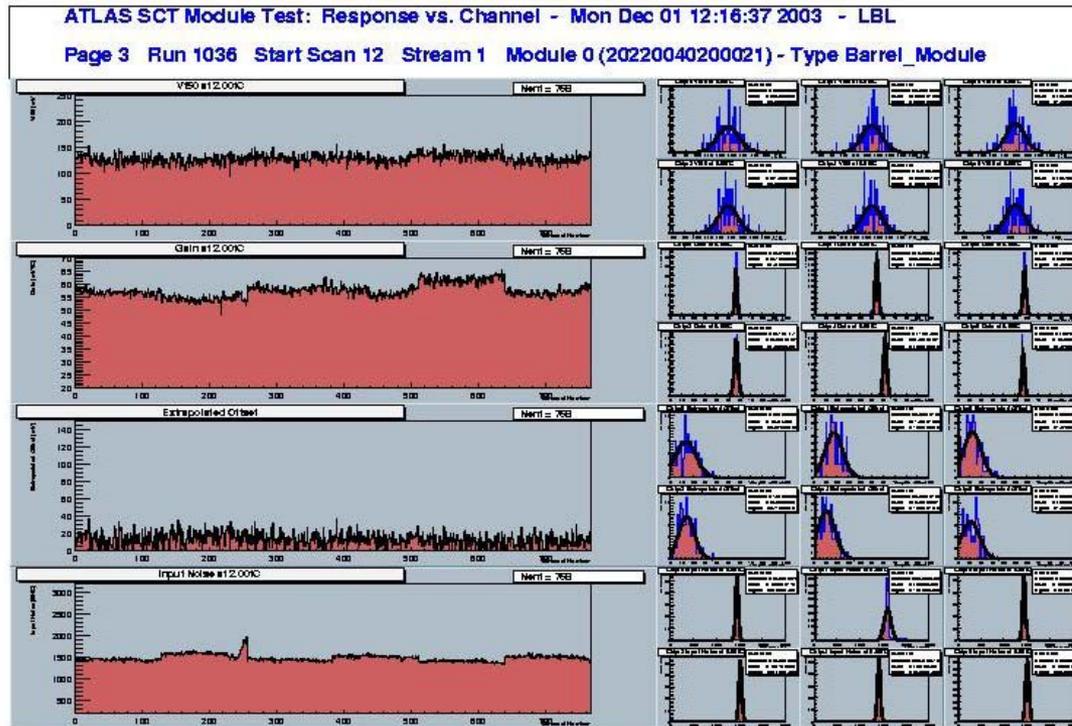


M8 S9 S10 S11 S12 E13  
20 22 22 21 21 19

# Module with BLG – 00021 - SD



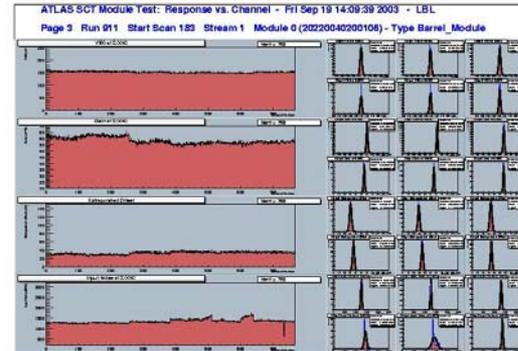
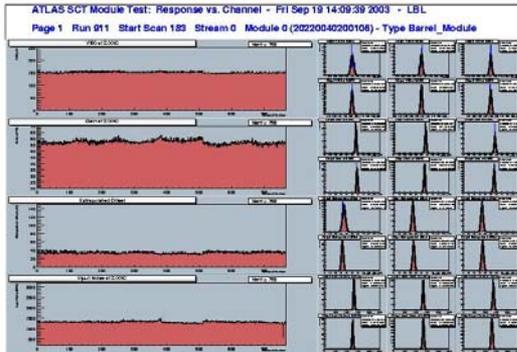
# Module with BLG – 00021 – SD 25%



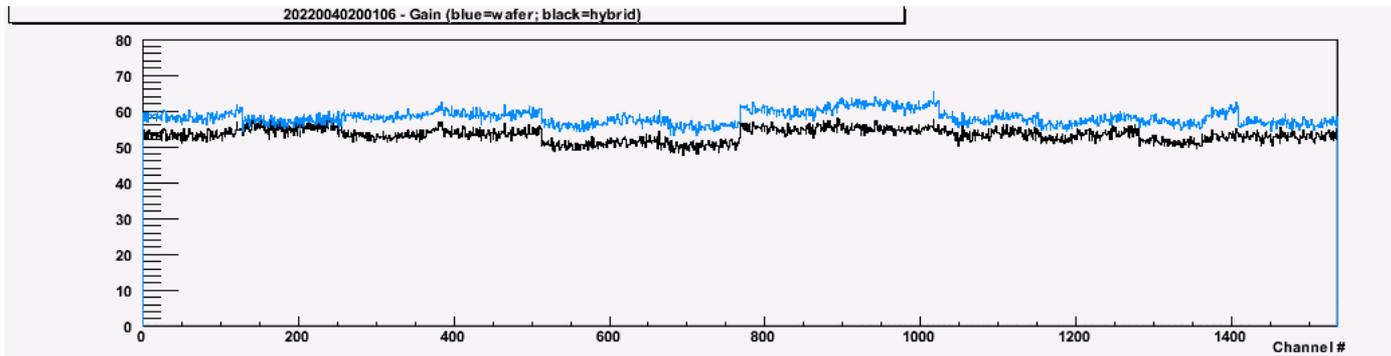
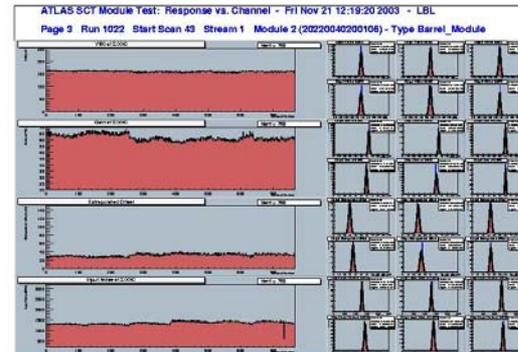
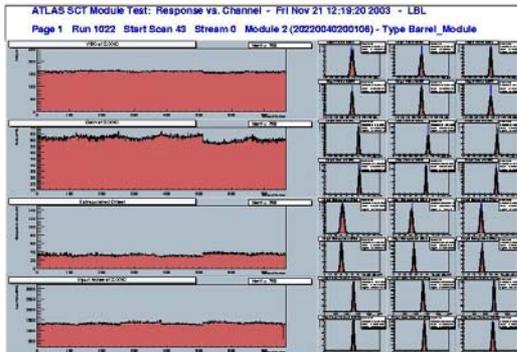
17 18 18 17 17 15

# Module with high noise - 00106

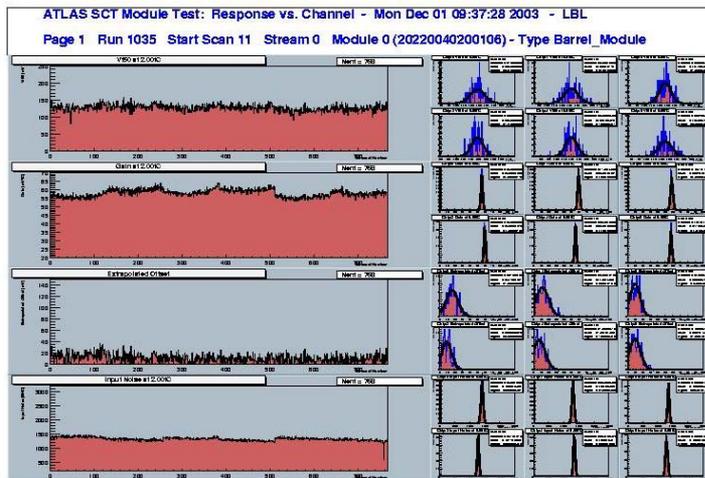
Module  
at cold



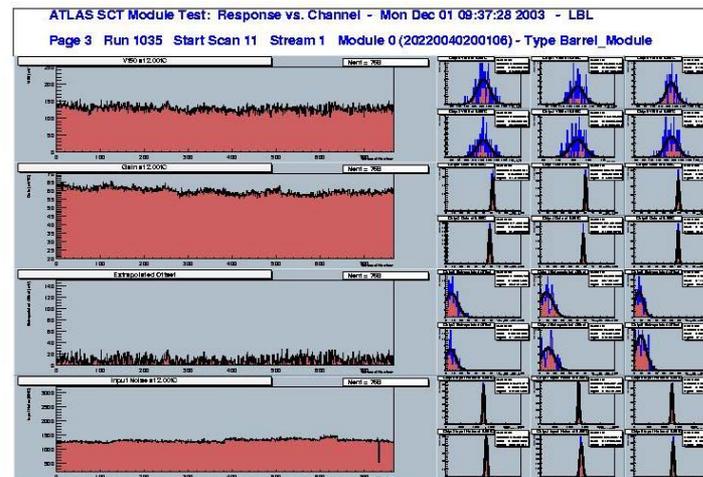
Module  
SD at 40%



# Module with high noise – 00106 SD 25%



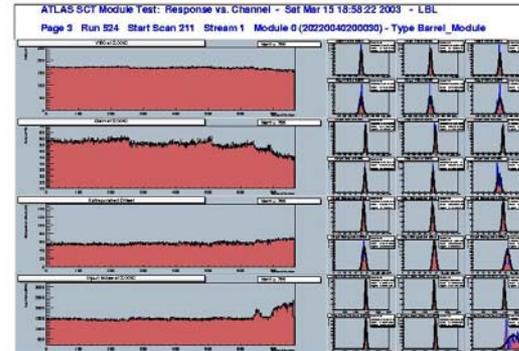
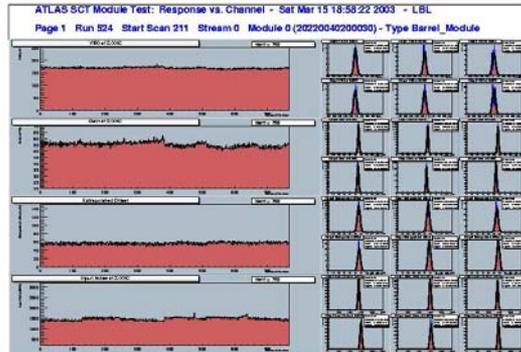
M0 S1 S2 S3 S4 E5  
 17 16 16 17 16 17



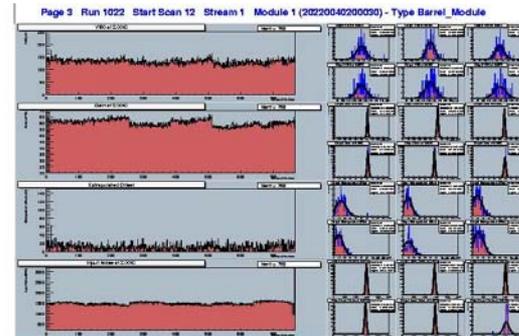
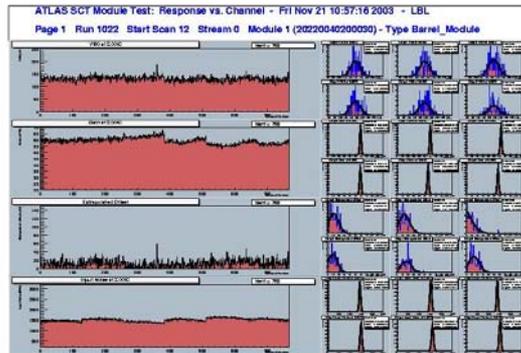
M8 S9 S10 S11 S12 E13  
 18 17 17 17 17 16

# Module with high noise - 00030

Module  
at cold

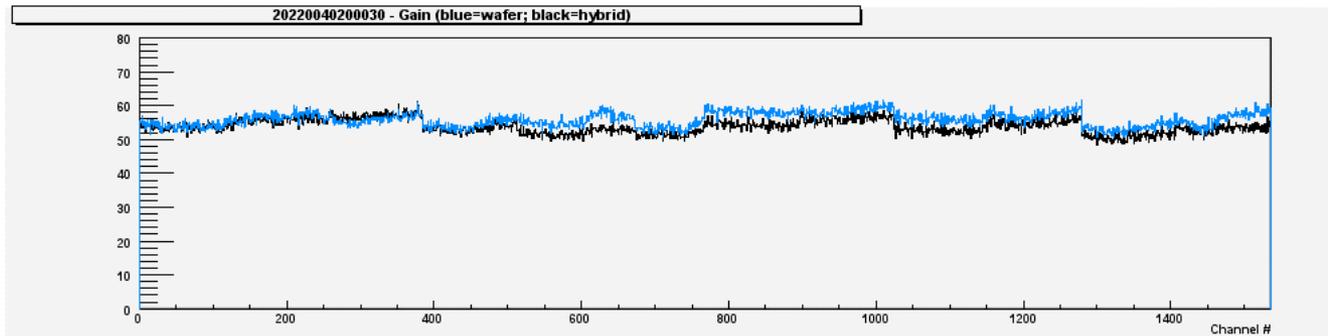


Module  
SD at 40%

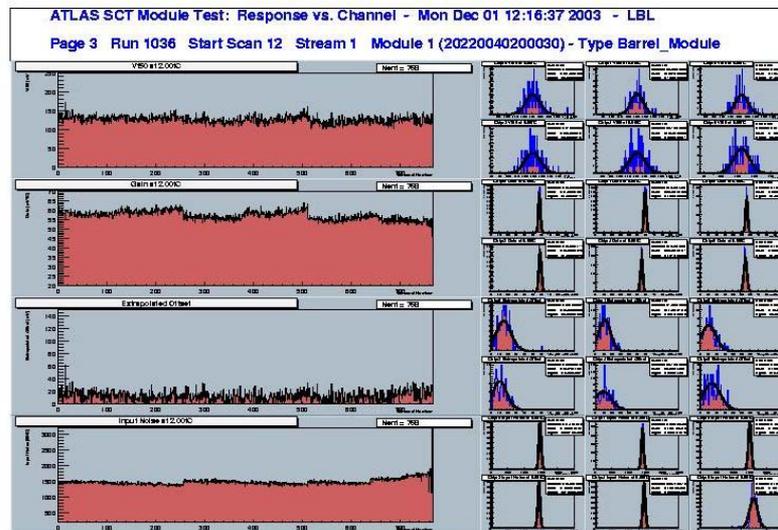
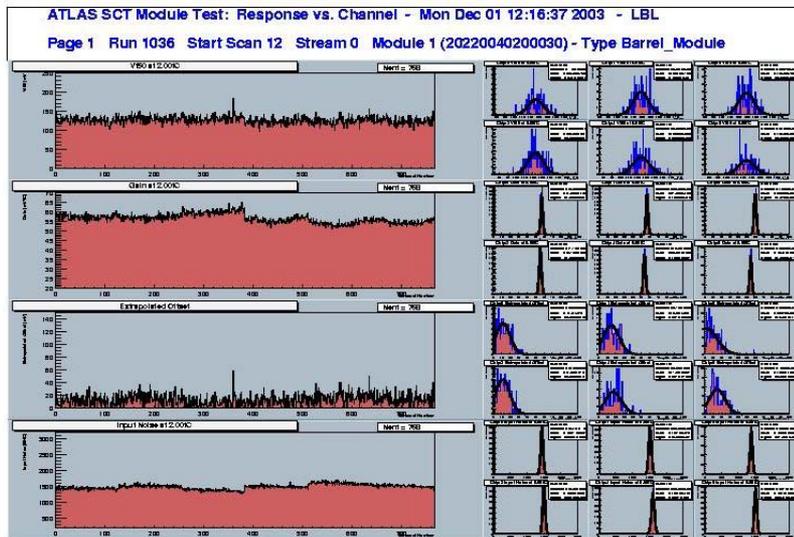


19 20 20 21 20 21

20 20 19 20 18 21



# Module with high noise – 00030 SD 25%



# Questions at DATA TAKING

- Automatic calibration of these ASIC's in the experiment
- The differences in timing should be accommodated in the 25ns time bucket
- Avoid low signals to slide into the next time bin

# Conclusions

- We have demonstrate that BLG chips are workable by increasing SD
- SD calculated with a complex algorithm desirable
- Module newly built (or already existing) with this effect or block of noisy channels become “good/pass” after applying the SD algorithm and 40% fraction (25% seems not to be always enough)
- Method could be refined and study is desirable to find the optimal SD fraction to use (30%?)
  
- Meanwhile we are happy to liberate the many hybrids on hold